
5648 User's Manual

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OCTAGON SYSTEMS CORPORATION®

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IMPORTANT!

Please read before installing your product.

Octagon's products are designed to be high in performance while consuming very little power. In order to maintain this advantage, CMOS circuitry is used.

CMOS chips have specific needs and some special requirements that the user must be aware of. Read the following to help avoid damage to your card from the use of CMOS chips.

Using CMOS Circuitry in Industrial Control

Industrial computers originally used LSTTL circuits. Because many PC components are used in laptop computers, IC manufacturers are exclusively using CMOS technology. Both TTL and CMOS have failure mechanisms, but they are different. This section describes some of the common failures which are common to all manufacturers of CMOS equipment. However, much of the information has been put in the context of the Micro PC.

Octagon has developed a reliable database of customer-induced, field failures. The average MTBF of Micro PC cards exceeds 11 years, yet there are failures. Most failures have been identified as customer-induced, but there is a small percentage that cannot be identified. As expected, virtually all the failures occur when bringing up the first system. On subsequent systems, the failure rate drops dramatically.

- Approximately 20% of the returned cards are problem-free. These cards, typically, have the wrong jumper settings or the customer has problems with the software. This causes frustration for the customer and incurs a testing charge from Octagon.
- Of the remaining 80% of the cards, 90% of these cards fail due to customer misuse and accident. Customers often cannot pinpoint the cause of the misuse.
- Therefore, 72% of the returned cards are damaged through some type of misuse. Of the remaining 8%, Octagon is unable to determine the cause of the failure and repairs these cards at no charge if they are under warranty.

The most common failures on CPU cards are over voltage of the power supply, static discharge, and damage to the serial and parallel ports. On expansion cards, the most common failures are static discharge, over voltage of inputs, over current of outputs, and misuse of the CMOS circuitry with regards to power supply sequencing. In the case of the video cards, the most common failure is to miswire the card to the flat panel display. Miswiring can damage both the card and an expensive display.

- **Multiple component failures** - The chance of a random component failure is very rare since the average MTBF of an Octagon card is greater than 11 years. In a 7 year study,

Octagon has never found a single case where multiple IC failures were not caused by misuse or accident. It is very probable that multiple component failures indicate that they were user-induced.

- **Testing “dead” cards** - For a card that is “completely nonfunctional”, there is a simple test to determine accidental over voltage, reverse voltage or other “forced” current situations. Unplug the card from the bus and remove all cables. Using an ordinary digital ohmmeter on the 2,000 ohm scale, measure the resistance between power and ground. Record this number. Reverse the ohmmeter leads and measure the resistance again. If the ratio of the resistances is 2:1 or greater, fault conditions most likely have occurred. A common cause is miswiring the power supply.
- **Improper power causes catastrophic failure** - If a card has had reverse polarity or high voltage applied, replacing a failed component is not an adequate fix. Other components probably have been partially damaged or a failure mechanism has been induced. Therefore, a failure will probably occur in the future. For such cards, Octagon highly recommends that these cards be replaced.
- **Other over-voltage symptoms** - In over-voltage situations, the programmable logic devices, EPROMs and CPU chips, usually fail in this order. The failed device may be hot to the touch. It is usually the case that only one IC will be overheated at a time.
- **Power sequencing** - The major failure of I/O chips is caused by the external application of input voltage while the Micro PC power is off. If you apply 5V to the input of a TTL chip with the power off, nothing will happen. Applying a 5V input to a CMOS card will cause the current to flow through the input and out the 5V power pin. This current attempts to power up the card. Most inputs are rated at 25 mA maximum. When this is exceeded, the chip may be damaged.
- **Failure on power-up** - Even when there is not enough current to destroy an input described above, the chip may be destroyed when the power to the card is applied. This is due to the fact that the input current biases the IC so that it acts as a forward biased diode on power-up. This type of failure is typical on serial interface chips.

-
- **Serial and parallel** - Customers sometimes connect the serial and printer devices to the Micro PC while the power is off. This can cause the failure mentioned in the above section, *Failure upon power-up*. Even if they are connected with the Micro PC on, there can be another failure mechanism. Some serial and printer devices do not share the same power (AC) grounding. The leakage can cause the serial or parallel signals to be 20-40V above the Micro PC ground, thus, damaging the ports as they are plugged in. This would not be a problem if the ground pin is connected first, but there is no guarantee of this. Damage to the printer port chip will cause the serial ports to fail as they share the same chip.
 - **Hot insertion** - Plugging cards into the card cage with the power on will usually not cause a problem. (**Octagon urges that you do not do this!**) However, the card may be damaged if the right sequence of pins contacts as the card is pushed into the socket. This usually damages bus driver chips and they may become hot when the power is applied. This is one of the most common failures of expansion cards.
 - **Using desktop PC power supplies** - Occasionally, a customer will use a regular desktop PC power supply when bringing up a system. Most of these are rated at 5V at 20A or more. Switching supplies usually require a 20% load to operate properly. This means 4A or more. Since a typical Micro PC system takes less than 2A, the supply does not regulate properly. Customers have reported that the output can drift up to 7V and/or with 7-8V voltage spikes. Unless a scope is connected, you may not see these transients.
 - **Terminated backplanes** - Some customers try to use Micro PC cards in backplanes that have resistor/capacitor termination networks. CMOS cards cannot be used with termination networks. Generally, the cards will function erratically or the bus drivers may fail due to excessive output currents.
 - **Excessive signal lead lengths** - Another source of failure that was identified years ago at Octagon was excessive lead lengths on digital inputs. Long leads act as an antenna to pick up noise. They can also act as unterminated transmission lines. When 5V is switch onto a line, it creates a transient waveform. Octagon has seen submicrosecond pulses of 8V or more. The solution is to place a capacitor, for example 0.1 μF , across the switch contact. This will also eliminate radio frequency and other high frequency pickup.
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PREFACE

This manual is a guide to the proper configuration and operation of your 5648 Analog/Digital Interface Card. Installation instructions, card mapping information and jumpering options are described in the main body of the manual; technical specifications are included in the appendices.

The 5648 card is designed to be used with any Octagon Micro PC Control Card. This combination provides a modular system which is easy to set up, modify and use. You can also use your 5648 in conjunction with other Micro PC expansion cards, allowing you to tailor your system for a wide variety of applications.

CONVENTIONS USED IN THIS MANUAL

1. Information which appears on your screen (output from your system or commands or data that you key in) is shown in a different type face.

Example 1:

```
Octagon 5648 ROM BIOS Vers X.XX  
Copyright (c) 1993, Octagon Systems, Corp.  
All rights reserved
```

Example 2:

Press the <ESC> key.

2. Italicized refers to information that is specific to your particular system or program, for example,

Enter *filename*

means enter the name of your file. Names of other sections or manuals are also italicized.

3. Warnings always appear in this format:

WARNING:

The warning message appears here.

-
4. Paired angle brackets are used to indicate a specific key on your keyboard, for example, <ESC> means the escape key; <CTRL> means the control key; <F1> means the F1 function key.
 5. All addresses are given in hexadecimal.

SYMBOLS AND TERMINOLOGY

Throughout this manual, the following symbols and terminology are used:

W[–] Denotes a jumper block and the pins to connect.

NOTE Information under this heading presents helpful tips for using the 5648.

WARNING:

Information under this heading warns you of situations which might cause catastrophic or irreversible damage.

PC SmartLINK A serial communications software package designed by Octagon. It provides communications between a PC and other equipment and may be used with any PC software package, including CAMBASIC IV. Refers to all versions of PC SmartLINK.

Reset Resetting the system hardware and software by pushing the reset switch. Has the same results as disconnecting power to the system, without the potential side effects of a cold reset.

TTL Compatible 0–5V logic levels.

H The suffix "H" denotes a hexadecimal number. For example, 1000H in hexadecimal equals 4096 in decimal.

TECHNICAL SUPPORT

If you have a question about the 5648 Analog/Digital Interface Card and can't find the answer in this manual, call Technical Support. They will be ready to give you the assistance you need.

When you call, please have the following at hand:

Your 5648 Analog/Digital Interface Card User's Manual

A description of your problem

The direct line to the Technical Support is 303-426-4521.

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DESCRIPTION

The Micro PC 5648 Analog/Digital Interface Card accepts switch closures and logic inputs, drives displays and LEDs, and interfaces with opto module racks. It also allows analog input and output modules to be mixed with digital I/O modules in the same opto isolator rack. Twenty-four of the 48 lines can be used for either analog or digital I/O, while the remaining 24 lines are digital I/O only. Each I/O line has a 22K pull-up resistor so that external resistors are not required when reading switch contacts. The card measures 4.5 x 4.9 inches and uses one slot of the Micro PC card cage. It is compatible with all Micro PC Control Cards and is electrically compatible with standard-sized CPU cards. It requires 5 volts at 270 mA typical.

The 5648 interfaces with most types of parallel devices, including LCD and VF displays, printers and single LEDs. The I/O levels are 0–5V and are compatible with standard TTL logic levels. If the field wiring requires termination, use the STB–26 with a CMA–26 cable.

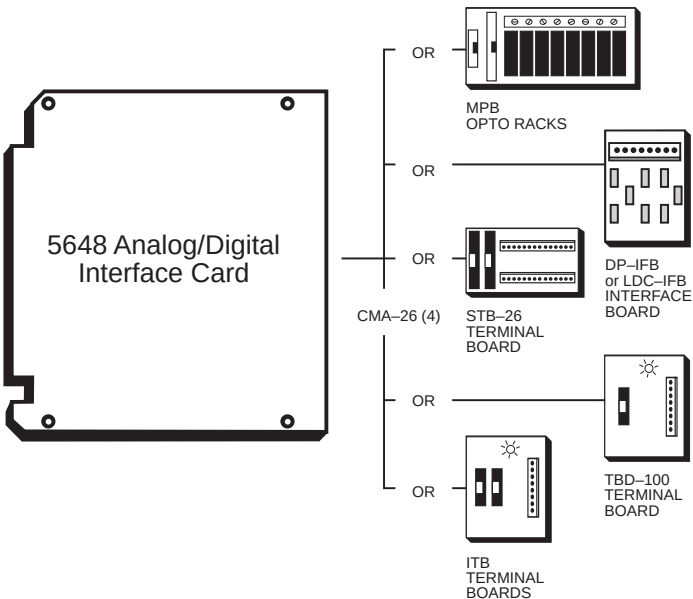


Figure 1–1—Typical 5648 system configuration

MAJOR FEATURES

Driving Opto Racks

The 5648 can drive up to two of the MPB-xx opto-module racks. The isolator modules are required when driving or receiving signals from high voltage and /or high current devices. Opto isolation also eliminates ground loops and significantly reduces the chance that noise will invade the system. The MPB-xx racks interface to the 5648 via CMA-26 cables.

Driving Analog I/O Modules

In addition to the standard digital I/O modules, the 5648 is compatible with Grayhill G5 modules. The G5 input modules produce a frequency output that is directly proportional to the input. A custom ASIC on the 5648 converts the frequency to a 0–4095 count. The commands from the CPU card select the channel and start the conversion. The ASIC generates an interrupt on the completion of the conversion. The maximum conversion time is 625 μ S.

The analog modules accept thermocouples, current loop, RTD and voltage inputs. Output modules include voltage and current outputs. The ASIC measures the frequency, eliminating processor overhead. The system will detect incorrect polarity, out-of-range signal, and missing or defective module conditions.

Driving Parallel Displays

Adapter cables are available for driving VF and LCD series displays. Software drivers are available. You can also drive almost any parallel display.

Access Indication

The 5648 has two LED indicators that flash briefly when each connector group of 24 is accessed. This is useful when debugging software.

The 5648 Analog/Digital Interface Card uses one slot of the Micro PC card cage. It may be used with any Micro PC Control Card.

NOTE: The G5 analog outputs will not work with the 508x Microcontrollers. The software utility disk does not apply.

WARNING:

The 5648 contains static sensitive CMOS components. The greatest danger occurs when the card is plugged into a card cage. The 5648 becomes charged by the user and the static discharges to the backplane from the pin closest to the card connector. If that pin happens to be an input pin, even TTL inputs may be damaged. To avoid damaging your card and its components:

- Ground yourself before handling the 5648 Digital I/O Card.
- Disconnect power before removing or inserting the 5648 Card.

EQUIPMENT

You will need the following equipment (or equivalent):

- 5648 Analog/Digital Interface Card
- Micro PC Control Card
- Micro PC Card Cage
- Power Supply or Module
- PC SmartLINK or other communications software.

INSTALLATION

Before installing the 5648 Analog/Digital Interface Card, refer to Figure 2-1 for the location of various connectors and jumpers and Figure 2-2 for a functional diagram of the card.

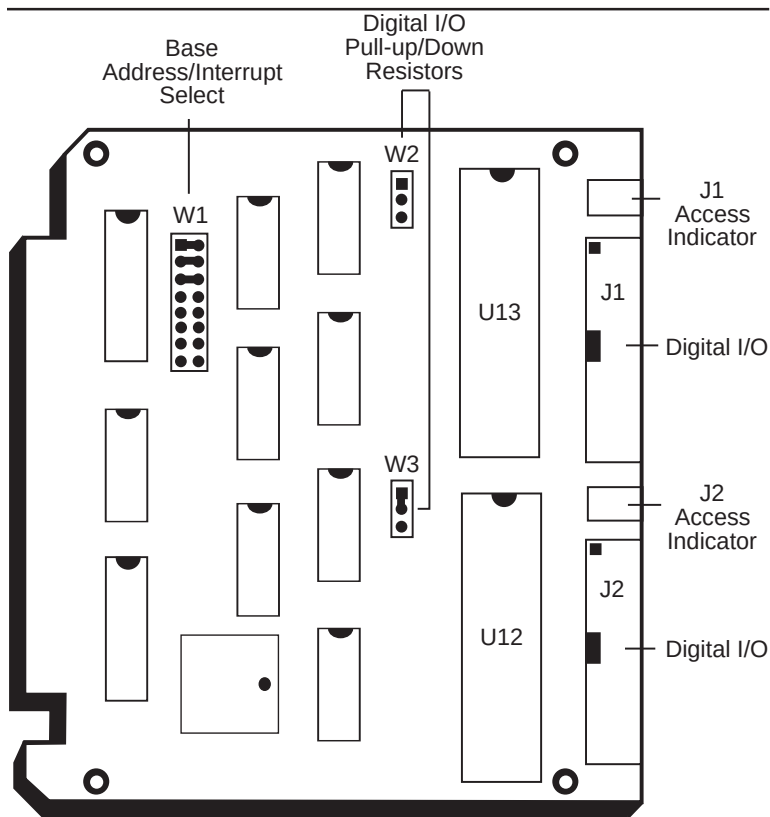


Figure 2-1—5648 Component Diagram

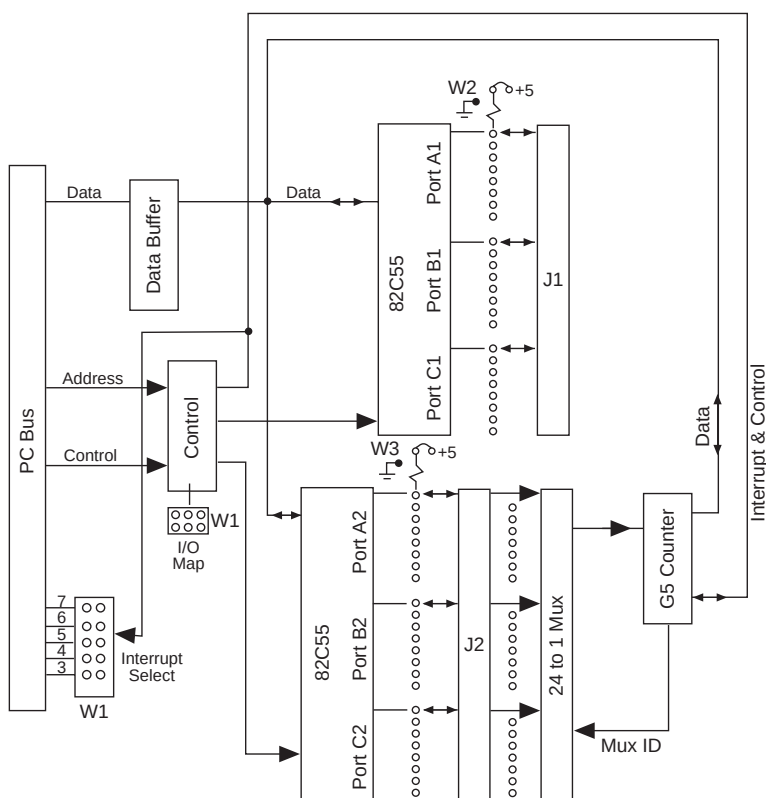


Figure 2-2—5648 Functional diagram

Base Address

The 5648 is configured at the factory to operate in most systems without any jumper changes. Jumper block W1 defines the base address. As shipped, the base address is 100H, which is jumper configuration W1[1–2, 3–4, 5–6]. If there is another card in your system with a base address of 100H, you must use a different base address for the 5648 or the other expansion card.

To change the base address, change the jumper connections in block W1:

Base Address Select: W1	
Pins Jumpered	Base Address
[1-2][3-4][5-6]	100H*
[3-4][5-6]	110H
[1-2][5-6]	120H
[5-6]	130H
[1-2][3-4]	140H
[3-4]	150H
[1-2]	160H
Not jumpered	170H

* = default

To install the 5648 in the card cage:

WARNING: Take care to correctly position the 5648 in the card cage. The V_{CC} and ground signals must match those on the backplane. Figure 2–3 shows the relative position of the 5648 as it is installed in the card cage.

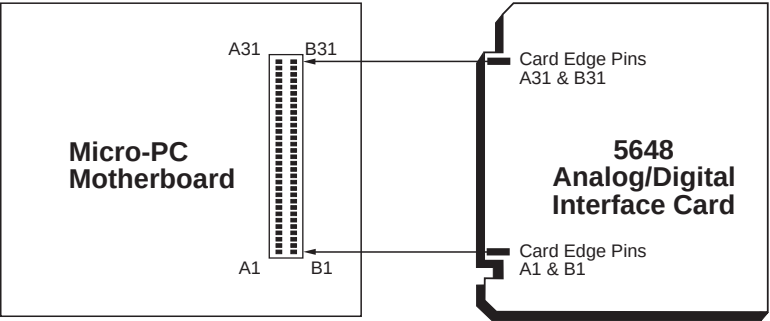


Figure 2–3—Edge Connector Orientation

-
1. Verify the base address settings are correct for your application.
 2. Make sure power to the card cage is OFF
.
 3. Slide the 5648 into the card cage. The components on the card should face to the left or up depending on the type of card cage.
 4. The amber LEDs will light briefly whenever the card is accessed (input or output) at J1 or J2

PORT PINOUTS

The pinouts are identical for connectors J1 and J2. Each connector has 24 I/O lines (3 ports), 5 volts and ground. The individual ports are designated A, B, and C. Port A has the lowest address; each half of port C is controllable (upper and lower C). Each port pin has a 22K pull-up/down resistor.

Digital I/O: J1 & J2			
Pin #	Function	Opto Position	
		J1	J2
19	Port A, line 0	8	8
21	Port A, line 1	9	9
23	Port A, line 2	10	10
25	Port A, line 3	11	11
24	Port A, line 4	12	12
22	Port A, line 5	13	13
20	Port A, line 6	14	14
18	Port A, line 7	15	15
10	Port B, line 0	16	16
8	Port B, line 1	17	17
4	Port B, line 2	18	18
6	Port B, line 3	19	19
1	Port B, line 4	20	20
3	Port B, line 5	21	21
5	Port B, line 6	22	22
7	Port B, line 7	23	23
13	Port C, line 0	0	0
16	Port C, line 1	1	1
15	Port C, line 2	2	2
17	Port C, line 3	3	3
14	Port C, line 4	4	4
11	Port C, line 5	5	5
12	Port C, line 6	6	6
9	Port C, line 7	7	7
2	+5V	NA	NA
26	Common		

DESCRIPTION

The 48 digital I/O lines on the 5648 are supplied by two 82C55 chips. The 82C55 located in U13 is connected to J1 and the 82C55 located in U12 is connected to J2. On power-up and software or hardware reset, all the digital I/O lines in J1 and J2 are configured as inputs. All lines are TTL logic level compatible (0–5V) and have 22K pull-up/down resistors to the 5V supply.

The 24 digital I/O lines at J1 and J2 can be used to interface to switches, turn on low-current LEDs, and other devices that have TTL input or output (for examples, printers and scales). The STB–26 terminal board provides a convenient way of interfacing switches or other digital I/O devices to the J1 and J2. A CMA–26 cable is used to interface the STB terminal board to the 5648. Digital I/O devices are then connected to the screw terminals on the STB–26. You can also connect opto-module racks and drive G4 opto-isolated and G5 analog modules. Figure 3–1 shows a typical terminal board and/or opto rack configuration.

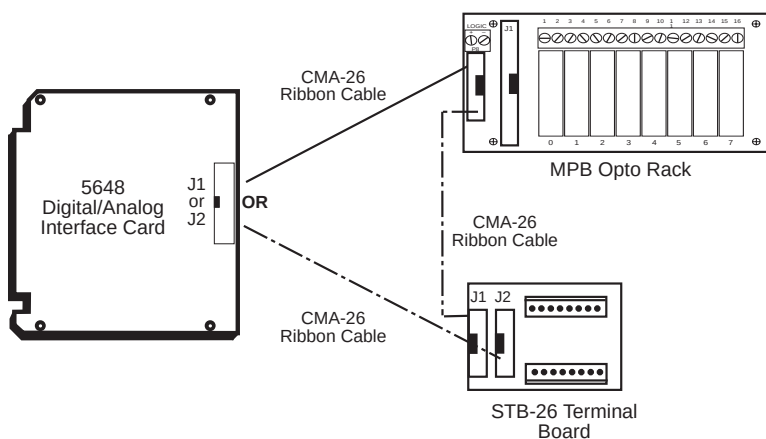


Figure 3–1—Typical Terminal Board and Opto Rack Configuration

PORT ADDRESSES

Each 82C55 has three ports with eight parallel I/O lines (bits) per port. Each port has a unique I/O address. Port A and Port B can be programmed as all inputs or all outputs. Port C can be programmed in one group of eight lines (all inputs or all outputs) or as two groups of four lines (upper and lower C). The four lines in upper or lower C can each be programmed as all inputs or all outputs:

5648 Digital I/O Port: J1 and J2			
Port	J1 I/O Address	J2 I/O Address	Description
A	1x0H	1x4H	8 lines which can be programmed as all inputs or all outputs
B	1x1H	1x5H	8 lines which can be programmed as all inputs or all outputs. 8 lines interface to a high current driver.
C	1x2H	1x6H	8 lines which can be programmed as one group of 8 lines or two groups of 4 lines as all inputs or all outputs.
Control Register	1x3H	1x7H	

NOTE: x is the value 0-7 depending on the base address selection at W1.

When a line is configured as an output, it can sink a maximum of 2.5 mA at 0.4V and can source over 2.5 mA at 2.4V. When driving opto-modules, the output can sink 15 mA at 1.0V.

The 5648 uses a block of 16 addresses. Refer to the following table for the function of the associated address:

Port Address Functions	
Function	Port Address
J1, Port A	Base + 00H
J1, Port B	Base + 01H
J1, Port C	Base + 02H
J1, Control Register	Base + 03H
J2, Port A	Base + 04H
J2, Port B	Base + 05H
J2, Port C	Base + 06H
J2, Control Register	Base + 07H
J2, G5 input start conversion, D7=1 (write); Counter Data Low (read)	Base + 08H
Reset Counter (write); Counter Data High (read)	Base + 09H
Channel Select Mux 1 of 24 (write); Channel Select Mux read back (read)	Base + 0AH
Status Register Interrupt, Bit 7=1; State Code, Bits 0-3; Value of 8FH=overflow	Base + 0BH

For a complete description of the capabilities of the 82C55, please refer to the information in Appendix A, in the Intel Peripheral Databook. Some of the chip's capabilities are described below.

CONFIGURING I/O LINES

On power-up or reset, all three ports are in the input state. You can alter which ports are inputs or outputs by writing a control command to the control register in the 82C55. The examples below assume the base address is 100H.

82C55 Control Register Commands					
HEX	DEC	Port A*	Port B*	Port UC*	Port LC*
80H	128	OUT	OUT	OUT	OUT
81H	129	OUT	OUT	OUT	IN
82H	130	OUT	IN	OUT	OUT
83H	131	OUT	IN	OUT	IN
88H	136	OUT	OUT	IN	OUT
89H	137	OUT	OUT	IN	IN
8AH	138	OUT	IN	IN	OUT
8BH	139	OUT	IN	IN	IN
90H	144	IN	OUT	OUT	OUT
91H	145	IN	OUT	OUT	IN
92H	146	IN	IN	OUT	OUT
93H	147	IN	IN	OUT	IN
98H	152	IN	OUT	IN	OUT
99H	153	IN	OUT	IN	IN
9AH	154	IN	IN	IN	OUT
9BH	155	IN	IN	IN	IN

* Ports A and B must be either all inputs of all outputs. Each half of Port C is controllable. Upper C (UC) includes bits 4 through 7 and Lower C (LC) includes bits 0 through 3.

Examples

The following example shows how to configure all three ports as outputs when the base address is set at 100H:

```
OUT  &H103, &H80
```

The following statement configures Ports A and C as input ports and B as an output port:

```
OUT  &H103, &H99
```

PULLING THE I/O LINES HIGH OR LOW

Jumper block W2 pulls all of the 24 I/O lines of the J1 high or low, while W3 affects the 24 I/O lines of J2. The factory default pulls all of the I/O lines high.

W2 & W3: Digital I/O Pull-up/Pull-down Resistors	
Pins Jumped	Description
[1-2]*	I/O lines pulled high
[2-3]	I/O lines pulled low

* = default

ACCESS INDICATOR LEDS

Two access indicators are on the 5648, one for each connector. When the lower 24 I/O lines of J1 are accessed, the J1 LED will flash. When the upper 24 I/O lines or the G5 input module hardware is accessed the J2 LED will flash.

DRIVING OPTO MODULE RACKS

The 5648 can drive two MPB-8, -16 or -24 series opto module racks via a CMA-26 cable interface. To drive opto module racks, plug one end of a CMA-26 cable into one of the J connectors that you want to use and the other end into the MPB opto mounting rack. Run ground and +5V to the opto mounting rack.

G4 Opto-isolated Modules

You can use G4 opto-isolated modules when driving or receiving signals from high voltage and/or high current devices. Opto-isolation also eliminates ground loops and significantly reduces the chance that noise will invade the system.

Use the following table to determine the corresponding opto channel for a particular 82C55 port. Remember to add the base address of the card.

Opto Channels			
Channel	82C55 Port	J1 Offset Address	J2 Offset Address
0-3	Lower C	2	6
4-7	Upper C	2	6
8-15	A	0	4
16-23	B	1	5

For example, if the base address of the 5648 is 110H, the following would be entered into the program:

A=INP(&H116) reads opto rack on J2, channels 0–7

G5 Analog Modules

OUTPUT

Ports A, B or C may be used on either J1 or J2 for G5 analog output. These ports must be configured as an output by writing to the control word register of the 82C55. Refer to the programming examples in the G5 directory on the 5648 utility disk for information on using G5 output modules. A file called README.DOC describes the demo programs and functions that are available in QuickBASIC and C. (Octagon's G5 analog output driver routines momentarily disables all interrupts while in use.)

NOTE: Because of strict timing requirements when updating the G5 output module, this feature is only available when the 5648 is used with the following Micro PC Control Cards: 5012, 5012A, 5025, 5025–486, 6012 and 6024.

INPUT

Only J2 may be used for G5 analog inputs. The frequency counter circuit used to read the G5 analog inputs is addressed at BASE + 8 through BASE + &HB. The steps for reading inputs are as follows:

- Reset frequency counter circuit
- Write multiplexer channel (0–23)

-
- Start the conversion
 - Wait until the conversion is completed
 - Read the counter data
 - Convert the counter data to 12-bit count

'The following is a sample program written in QuickBASIC V4.5
'This program reads a G5 input module connected to an 'off-card'
'opto rack. If you run this program without a video card, substitute
'the PRINT statement with the PRINTS function included on the
5648 utility disk. The 5648 is mapped to 100H.

```
DEFINT A-Z                                'use integers where possible
ZC# = 250000/9                            'zero offset factor
G5BASE = &H108                           'base address of counter
OUT &H107, &H9B                           'config 8255 port C as inputs
FOR X = 1 TO 1000                         'take 1000 samples
    OUT G5BASE + 1, 0                     'reset freq. counter
    OUT G5BASE + 2, 8                     'select G5 channel #8
    OUT G5BASE, &H80                     'start conversion
    WHILE (INP(G5BASE + 3) < &H7F)      'poll until conv done
    WEND
    LSB& = INP(G5BASE)                   'read count lsb
    MSB& = INP(G5BASE + 1)               'read count msb
    WORD& = LSB& + (MSB& * 256)         'form the word
    VALUE=INT(((ZC#-WORD&)/(WORD&/1024))+.5) 'scale value
    PRINT VALUE
NEXT X
END
```

The conversion time will be less than 1 mS maximum. The End of Conversion may be determined either by using an interrupt or by polling the status register. In the event that a conversion is started on a channel that is not connected to a G5 module, the counting circuit will time out with a count value of 7FFFH. The data that is read is contained in 15 bits. The most significant bit of the high data byte will always be a zero. The data that is read must be converted to a numeric value in the range of 0 to 4095 as per the above program example.

NOTE: The utility disk also includes software drivers that can be used to read G5 input modules. Descriptions of the drivers are included in the README.DOC file.

You may optionally configure the 5648 to generate an interrupt at the end of each conversion (versus polling). Use the W1 jumper block to define the interrupt number.

Interrupt Select: W1	
Pins Jumpered	Interrupt
[7-8]	3
[9-10]	4
[11-12]	5
[13-14]	6
[15-16]	7
[8-10]*	No interrupts

* = default

TROUBLESHOOTING

If you have difficulty getting your system to work properly, remove all expansion cards except the 5648 Digital/Analog Interface Card from your system and check the power module and jumper configurations.

Power Module

The power module voltage should be $5V \pm 0.25V$ when measured at the connector pins. The power module ripple should be less than 50 mV.

Jumper Configuration

The 5648 is shipped with jumper connections in place for Base I/O Address 100H. Jumper changes are usually not needed to get the system running. If you changed the jumpers and the system is not working properly, return the system to the original jumper positions. If you still encounter difficulties, please contact Technical Support at 303-426-4521.

TECHNICAL SPECIFICATIONS

The 5648 accepts switch closures and logic inputs; drives displays and LEDs; and interfaces with opto mounting racks. Each I/O line has a 22K pull-up/down resistor; external resistors are not required when using switch contacts. The 5648 will interface with most parallel devices, including LCD and DP (vacuum fluorescent) series displays, printers, and single LEDs. The I/O levels are 0–5 volts and are compatible with standard TTL logic levels.

DC Characteristics

Input Low: -0.3V to $+0.8\text{V}$.

Input High: 2V to V_{cc} .

Output Low: 0.45V maximum.

Output High: 2.4V minimum.

Connectors

Two male 26-position, straight I/O connectors (Ansley #609–1007). Mates with Octagon CMA–26 cable.

Opto Rack Interface

Directly drives Octagon MPB series opto racks using CMA–26 cable. Drives G4 opto-isolated and G5 analog modules.

Software Support

Software drivers are provided on the 5648 utility disk. A README.DOC text file explains the driver usages.

Bus Compatibility

Electrically compatible with the PC bus; designed to be used in the Micro PC card cage with Octagon's Micro PC Control Cards. May be used with AT-sized PC's if used in conjunction with adapter bracket.

Power Requirements

$5\text{V} \pm 5\%$ at 270 mA typical, 300 mA maximum.

Environmental

-40° to 70°C operating temperature; -50° to 85°C nonoperating
5 to 95% RH, noncondensing

Size

4.5 in. x 4.9 in.

I/O MAP

Port Address Functions	
Function	Port Address
J1, Port A	Base + 00H
J1, Port B	Base + 01H
J1, Port C	Base + 02H
J1, Control Register	Base + 03H
J2, Port A	Base + 04H
J2, Port B	Base + 05H
J2, Port C	Base + 06H
J2, Control Register	Base + 07H
J2, G5 input start conversion, D7=1 (write); Counter Data Low (read)	Base + 08H
Reset Counter (write); Counter Data High (read)	Base + 09H
Channel Select Mux 1 of 24 (write); Channel Select Mux read back (read)	Base + 0AH
Status Register Interrupt, Bit 7=1; State Code, Bits 0-3; Value of 8FH=overflow	Base + 0BH

JUMPER CONFIGURATIONS

Base Address Select: W1	
Pins Jumpered	Base Address
[1-2][3-4][5-6]	100H*
[3-4][5-6]	110H
[1-2][5-6]	120H
[5-6]	130H
[1-2][3-4]	140H
[3-4]	150H
[1-2]	160H
Not jumpered	170H

* = default

Interrupt Select: W1	
Pins Jumpered	Interrupt
[7-8]	3
[9-10]	4
[11-12]	5
[13-14]	6
[15-16]	7
[8-10]*	No interrupts

* = default

W2 & W3: Digital I/O Pull-up/Pull-down Resistors	
Pins Jumpered	Description
[1-2]*	I/O lines pulled high
[2-3]	I/O lines pulled low

* = default

CONNECTOR PINOUTS

Digital I/O: J1 & J2			
Pin #	Function	Opto Position	
		J1	J2
19	Port A, line 0	8	8
21	Port A, line 1	9	9
23	Port A, line 2	10	10
25	Port A, line 3	11	11
24	Port A, line 4	12	12
22	Port A, line 5	13	13
20	Port A, line 6	14	14
18	Port A, line 7	15	15
10	Port B, line 0	16	16
8	Port B, line 1	17	17
4	Port B, line 2	18	18
6	Port B, line 3	19	19
1	Port B, line 4	20	20
3	Port B, line 5	21	21
5	Port B, line 6	22	22
7	Port B, line 7	23	23
13	Port C, line 0	0	0
16	Port C, line 1	1	1
15	Port C, line 2	2	2
17	Port C, line 3	3	3
14	Port C, line 4	4	4
11	Port C, line 5	5	5
12	Port C, line 6	6	6
9	Port C, line 7	7	7
2	+5V	NA	NA
26	Common		

Appendix A Intel 82C55 Data Sheet

INTEL 82C55A DATA SHEET

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82C55A CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- Compatible with all Intel and Most Other Microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5 mA DC Drive Capability on all I/O Port Outputs
- Available in 40-Pin DIP and 44-Pin PLCC
- Available in EXPRESS
 - Standard Temperature Range
 - Extended Temperature Range

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

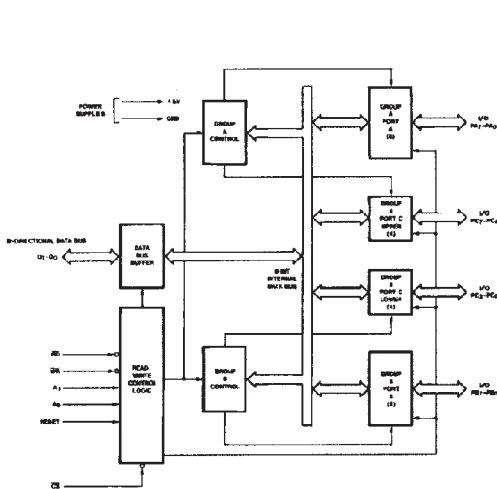
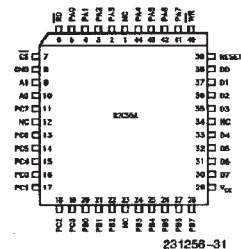
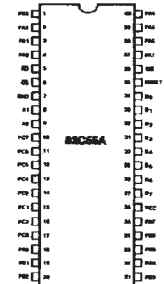


Figure 1. 82C55A Block Diagram

231256-1



231256-31



231256-2

Figure 2. 82C55A Pinout
Diagrams are for pin reference only. Package sizes are not to scale.

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© INTEL CORPORATION, 1992

Order Number: 231256-004

Table 1. Pin Description

Symbol	Pin Number Dip	PLCC	Type	Name and Function																																																																														
PA ₃₋₀	1-4	2-5	I/O	PORT A, PINS 0-3: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.																																																																														
RD	5	6	I	READ CONTROL: This input is low during CPU read operations.																																																																														
CS	6	7	I	CHIP SELECT: A low on this input enables the 82C55A to respond to RD and WR signals. RD and WR are ignored otherwise.																																																																														
GND	7	8		System Ground																																																																														
A ₁₋₀	8-9	9-10	I	ADDRESS: These input signals, in conjunction RD and WR, control the selection of one of the three ports or the control word registers. <table><tr><td>A₁</td><td>A₀</td><td>RD</td><td>WR</td><td>CS</td><td>Input Operation (Read)</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr><tr><td colspan="6">Output Operation (Write)</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr><tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr><tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Control</td></tr><tr><td colspan="6">Disable Function</td></tr><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>Data Bus - 3 - State</td></tr><tr><td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>Data Bus - 3 - State</td></tr></table>	A ₁	A ₀	RD	WR	CS	Input Operation (Read)	0	0	0	1	0	Port A - Data Bus	0	1	0	1	0	Port B - Data Bus	1	0	0	1	0	Port C - Data Bus	1	1	0	1	0	Control Word - Data Bus	Output Operation (Write)						0	0	1	0	0	Data Bus - Port A	0	1	1	0	0	Data Bus - Port B	1	0	1	0	0	Data Bus - Port C	1	1	1	0	0	Data Bus - Control	Disable Function						X	X	X	X	1	Data Bus - 3 - State	X	X	1	1	0	Data Bus - 3 - State
A ₁	A ₀	RD	WR	CS	Input Operation (Read)																																																																													
0	0	0	1	0	Port A - Data Bus																																																																													
0	1	0	1	0	Port B - Data Bus																																																																													
1	0	0	1	0	Port C - Data Bus																																																																													
1	1	0	1	0	Control Word - Data Bus																																																																													
Output Operation (Write)																																																																																		
0	0	1	0	0	Data Bus - Port A																																																																													
0	1	1	0	0	Data Bus - Port B																																																																													
1	0	1	0	0	Data Bus - Port C																																																																													
1	1	1	0	0	Data Bus - Control																																																																													
Disable Function																																																																																		
X	X	X	X	1	Data Bus - 3 - State																																																																													
X	X	1	1	0	Data Bus - 3 - State																																																																													
PC ₇₋₄	10-13	11,13-15	I/O	PORT C, PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.																																																																														
PC ₀₋₃	14-17	16-19	I/O	PORT C, PINS 0-3: Lower nibble of Port C.																																																																														
PB ₀₋₇	18-25	20-22, 24-28	I/O	PORT B, PINS 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer.																																																																														
V _{CC}	26	29		SYSTEM POWER: + 5V Power Supply.																																																																														
D ₇₋₀	27-34	30-33, 35-38	I/O	DATA BUS: Bi-directional, tri-state data bus lines, connected to system data bus.																																																																														
RESET	35	39	I	RESET: A high on this input clears the control register and all ports are set to the input mode.																																																																														
WR	36	40	I	WRITE CONTROL: This input is low during CPU write operations.																																																																														
PA ₇₋₄	37-40	41-44	I/O	PORT A, PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.																																																																														
NC		1, 12, 23, 34		No Connect																																																																														

82C55A FUNCTIONAL DESCRIPTION

General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7-C4)
Control Group B - Port B and Port C lower (C3-C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

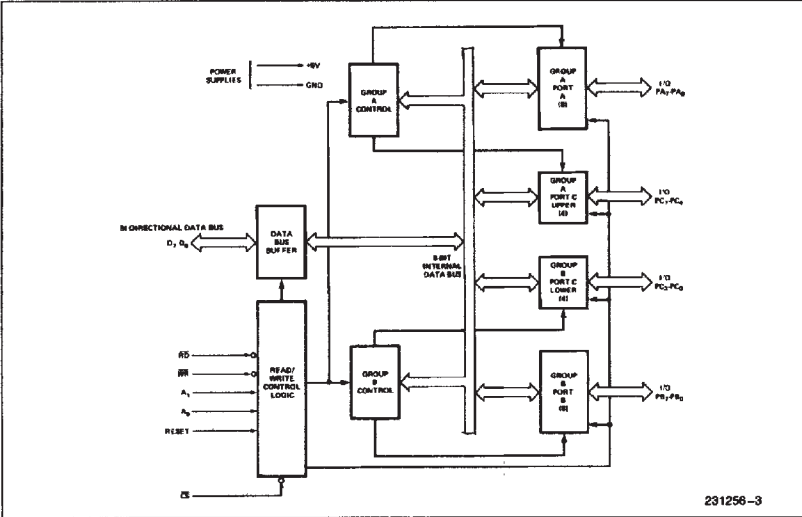


Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

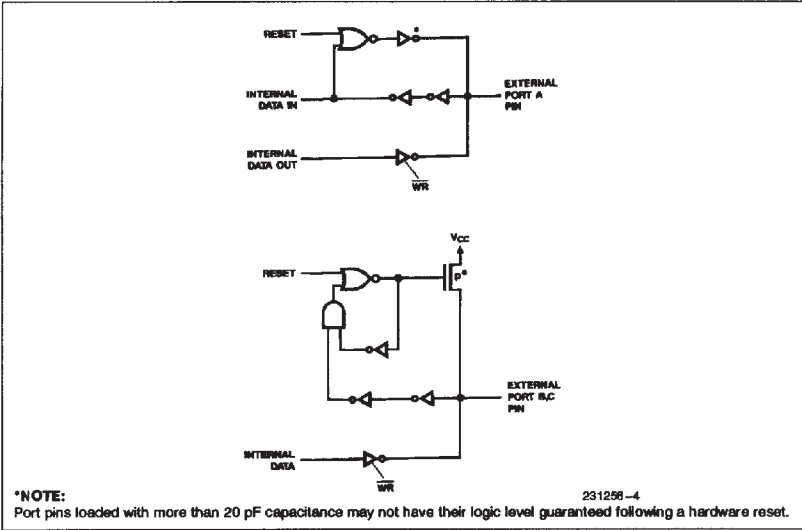


Figure 4. Port A, B, C, Bus-hold Configuration

82C55A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

- Mode 0 — Basic input/output
- Mode 1 — Strobed Input/output
- Mode 2 — Bi-directional Bus

When the reset input goes "high" all ports will be set to the input mode with all 24 port lines held at a logic "one" level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

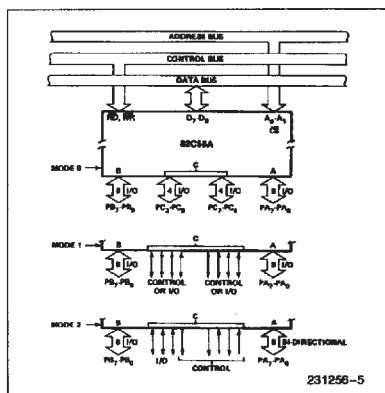


Figure 5. Basic Mode Definitions and Bus Interface

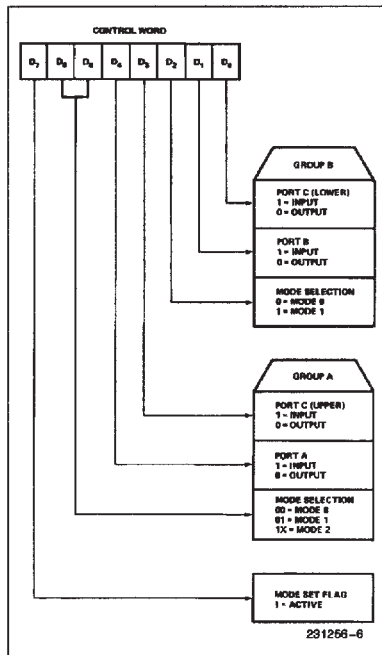


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTPUT instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

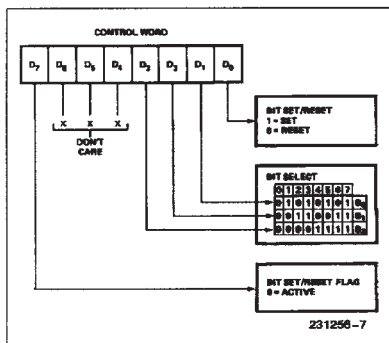


Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET)—INTE is SET—Interrupt enable

(BIT-RESET)—INTE is RESET—Interrupt disable

Note:

All Mask flip-flops are automatically reset during mode selection and device Reset.

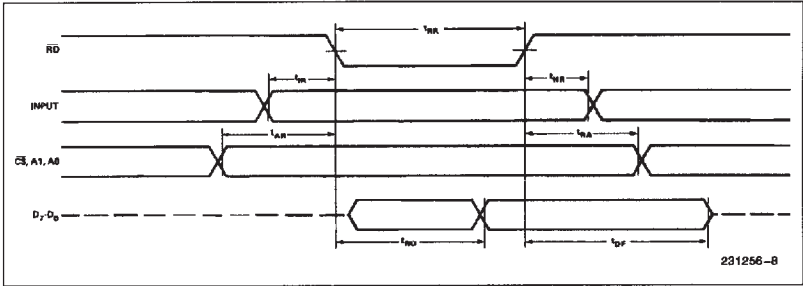
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

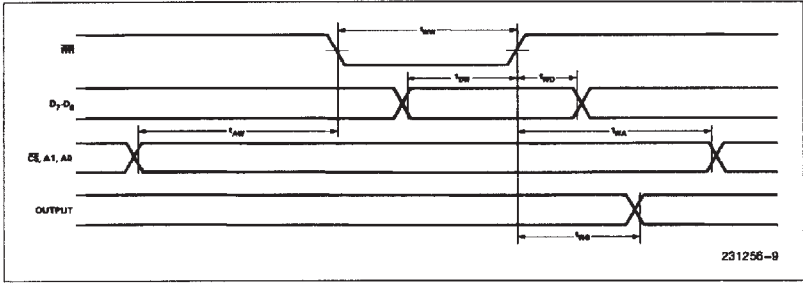
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



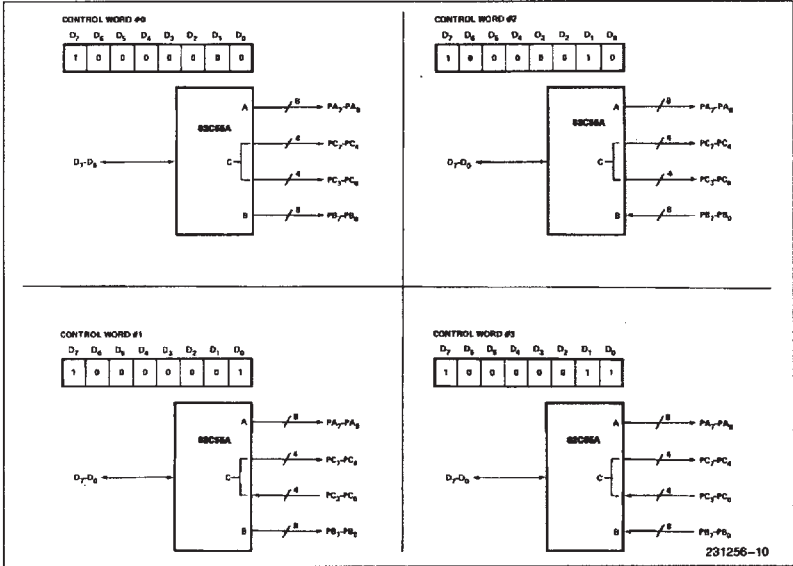
MODE 0 (BASIC OUTPUT)



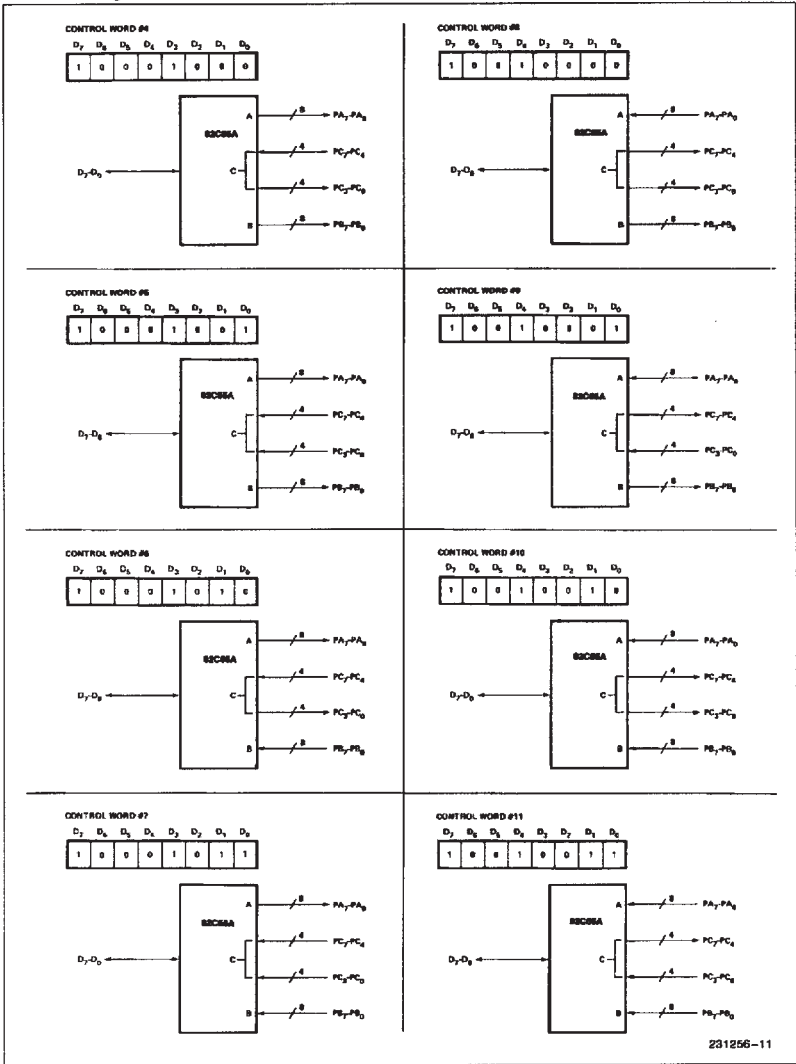
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D ₄	D ₃	D ₁	D ₀	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

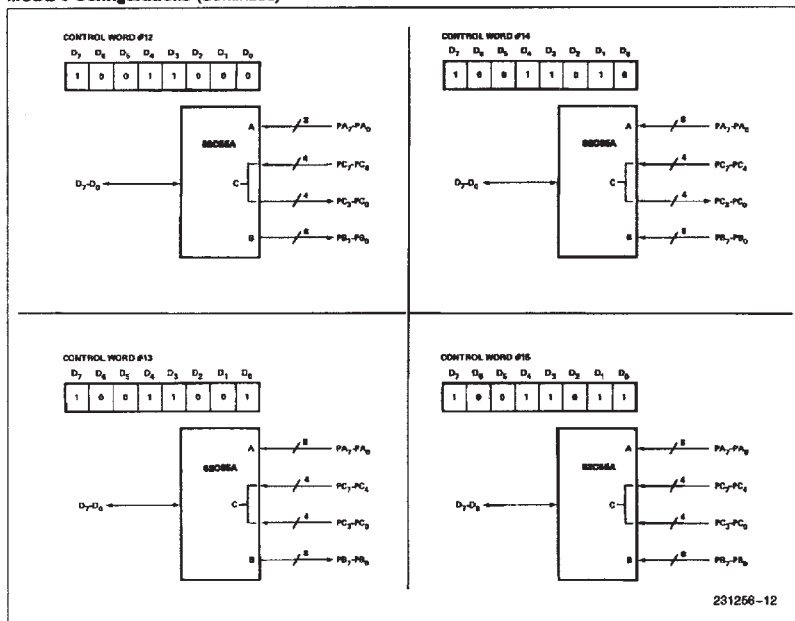


MODE 0 Configurations (Continued)



231256-11

MODE 0 Configurations (Continued)



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the STB is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of RD. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC₄.

INTE B

Controlled by bit set/reset of PC₂.

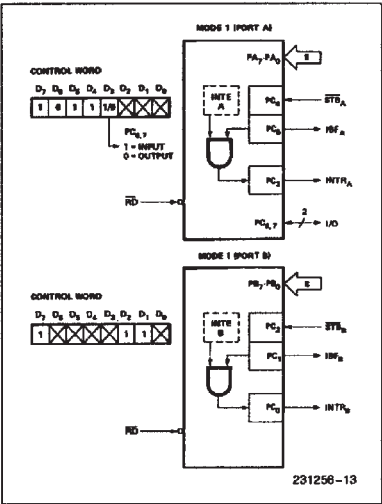


Figure 8. MODE 1 Input

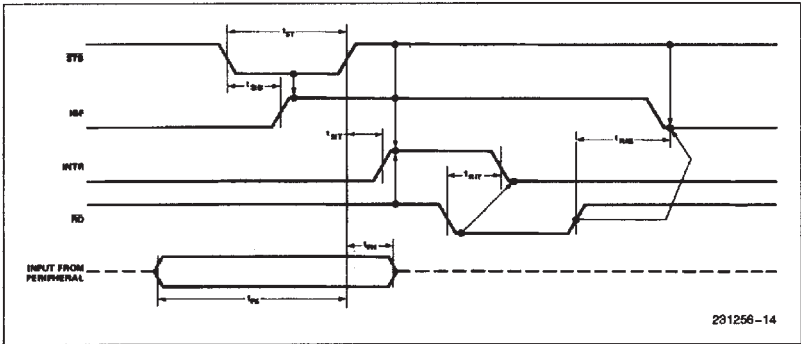


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

OBF (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK input being low.

ACK (Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC₆.

INTE B

Controlled by bit set/reset of PC₂.

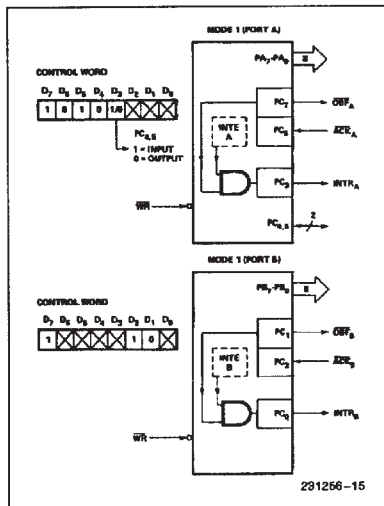


Figure 10. MODE 1 Output

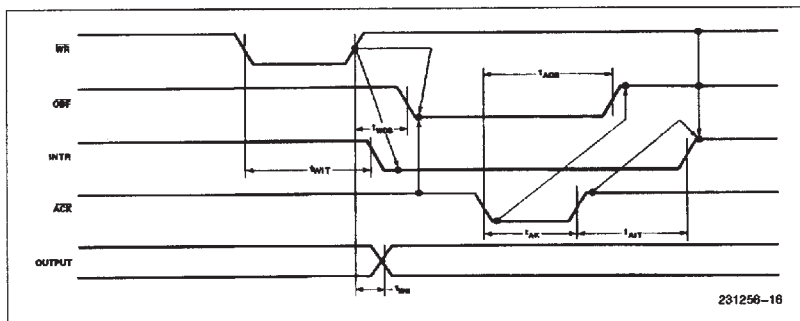


Figure 11. MODE 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

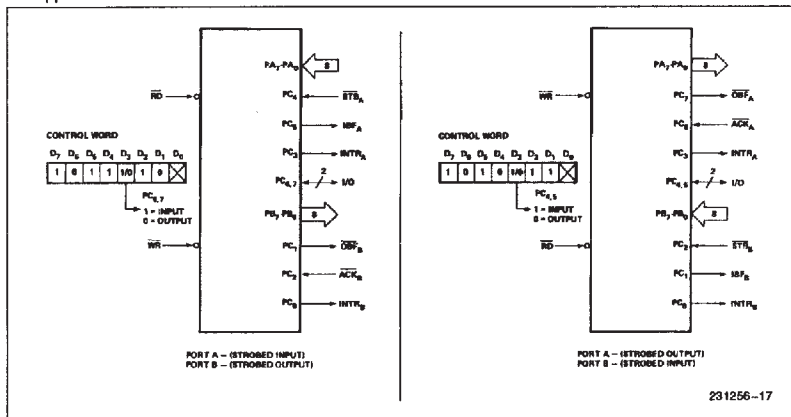


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5-bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

OBF (Output Buffer Full). The OBF output will go "low" to indicate that the CPU has written data out to port A.

ACK (Acknowledge). A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC₆.

Input Operations

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC₄.

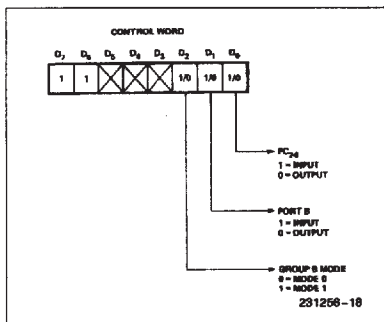


Figure 13. MODE Control Word

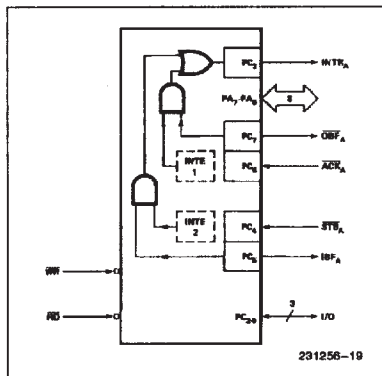


Figure 14. MODE 2

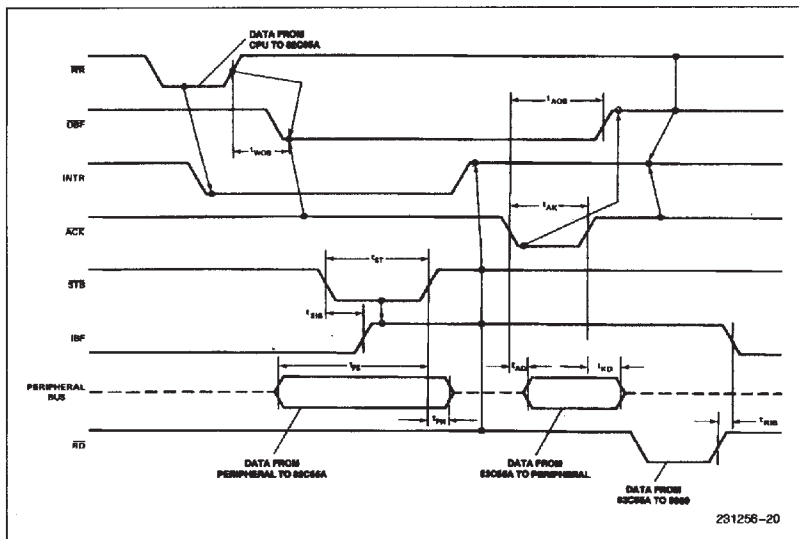
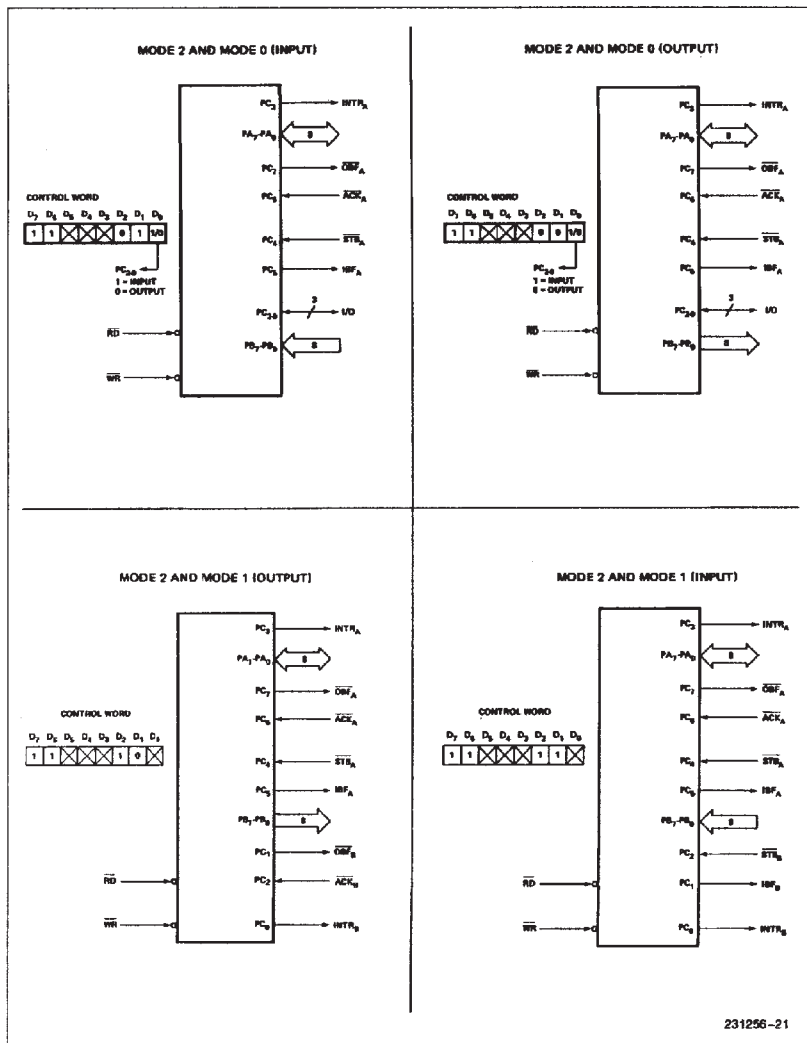


Figure 15. MODE 2 (Bidirectional)

NOTE:

Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
 $(INTR = IBF \cdot MASK \cdot STB \cdot RD + OBF \cdot MASK \cdot ACK \cdot WR)$



Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA ₀	IN	OUT	IN	OUT	↔	
PA ₁	IN	OUT	IN	OUT	↔	
PA ₂	IN	OUT	IN	OUT	↔	
PA ₃	IN	OUT	IN	OUT	↔	
PA ₄	IN	OUT	IN	OUT	↔	
PA ₅	IN	OUT	IN	OUT	↔	
PA ₆	IN	OUT	IN	OUT	↔	
PA ₇	IN	OUT	IN	OUT	↔	
PB ₀	IN	OUT	IN	OUT	—	
PB ₁	IN	OUT	IN	OUT	—	
PB ₂	IN	OUT	IN	OUT	—	
PB ₃	IN	OUT	IN	OUT	—	
PB ₄	IN	OUT	IN	OUT	—	
PB ₅	IN	OUT	IN	OUT	—	
PB ₆	IN	OUT	IN	OUT	—	
PB ₇	IN	OUT	IN	OUT	—	
PC ₀	IN	OUT	INTR _B	INTR _B	I/O	
PC ₁	IN	OUT	IBF _B	OBFB _B	I/O	
PC ₂	IN	OUT	STB _B	ACK _B	I/O	
PC ₃	IN	OUT	INTR _A	INTR _A	INTR _A	
PC ₄	IN	OUT	STB _A	I/O	STB _A	
PC ₅	IN	OUT	IBF _A	I/O	IBF _A	
PC ₆	IN	OUT	I/O	ACK _A	ACK _A	
PC ₇	IN	OUT	I/O	OBFA _A	OBFA _A	

MODE 0
OR MODE 1
ONLY

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the ACK and STB lines, will be placed on the data bus. In place of the ACK and STB line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to

change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and OBF) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including ACK and STB lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the ACK and STB lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5 mA. This feature allows the 82C55A to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

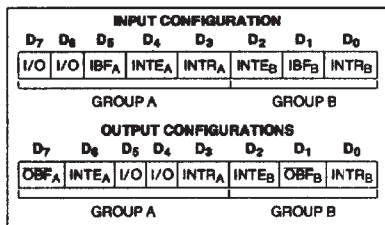


Figure 17a. MODE 1 Status Word Format

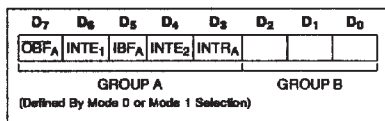


Figure 17b. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	ACK _B (Output Mode 1) or STB _B (Input Mode 1)
INTE A2	PC4	STB _A (Input Mode 1 or Mode 2)
INTE A1	PC6	ACK _A (Output Mode 1 or Mode 2)

Figure 18. Interrupt Enable Flags in Modes 1 and 2

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to + 70°C
 Storage Temperature - 65°C to + 150°C
 Supply Voltage - 0.5 to + 8.0V
 Operating Voltage + 4V to + 7V
 Voltage on any Input GND - 2V to + 6.5V
 Voltage on any Output GND - 0.5V to V_{CC} + 0.5V
 Power Dissipation 1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, GND = 0V (T_A = -40°C to +85°C for Extended Temperature)

Symbol	Parameter	Min	Max	Units	Test Conditions
V _{IL}	Input Low Voltage	-0.5	0.8	V	
V _{IH}	Input High Voltage	2.0	V _{CC}	V	
V _{OL}	Output Low Voltage		0.4	V	I _{OL} = 2.5 mA
V _{OH}	Output High Voltage	3.0 V _{CC} - 0.4		V V	I _{OH} = -2.5 mA I _{OH} = -100 µA
I _{IL}	Input Leakage Current		± 1	µA	V _{IN} = V _{CC} to 0V (Note 1)
I _{OFL}	Output Float Leakage Current		± 10	µA	V _{IN} = V _{CC} to 0V (Note 2)
I _{DAR}	Darlington Drive Current	± 2.5	(Note 4)	mA	Ports A, B, C R _{ext} = 500Ω V _{ext} = 1.7V
I _{PHL}	Port Hold Low Leakage Current	+ 50	+ 300	µA	V _{OUT} = 1.0V Port A only
I _{PHH}	Port Hold High Leakage Current	- 50	- 300	µA	V _{OUT} = 3.0V Ports A, B, C
I _{PHLO}	Port Hold Low Overdrive Current	- 350		µA	V _{OUT} = 0.8V
I _{PHHO}	Port Hold High Overdrive Current	+ 350		µA	V _{OUT} = 3.0V
I _{CC}	V _{CC} Supply Current		10	mA	(Note 3)
I _{CCSB}	V _{CC} Supply Current-Standby		10	µA	V _{CC} = 5.5V V _{IN} = V _{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low CS = High Reset = Low Pure Inputs = Low/High

NOTES:

1. Pins A₁, A₀, CS, WR, RD, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.

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CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CC} = \text{GND} = 0\text{V}$

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND $f_c = 1\text{ MHz}^{(5)}$
$C_{I/O}$	I/O Capacitance		20	pF	

NOTE:

5. Sampled not 100% tested.

A.C. CHARACTERISTICS

$T_A = 0^\circ$ to 70°C , $V_{CC} = +5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}$

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ for Extended Temperature

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AR}	Address Stable Before $\text{RD} \downarrow$	0		ns	
t_{RA}	Address Hold Time After $\text{RD} \uparrow$	0		ns	
t_{RR}	RD Pulse Width	150		ns	
t_{RD}	Data Delay from $\text{RD} \downarrow$		120	ns	
t_{DF}	$\text{RD} \uparrow$ to Data Floating	10	75	ns	
t_{RV}	Recovery Time between RD/WR	200		ns	

WRITE CYCLE

Symbol	Parameter	82C55A-2		Units	Test Conditions
		Min	Max		
t_{AW}	Address Stable Before $\text{WR} \downarrow$	0		ns	
t_{WA}	Address Hold Time After $\text{WR} \uparrow$	20		ns	Ports A & B
		20		ns	Port C
t_{WW}	WR Pulse Width	100		ns	
t_{DW}	Data Setup Time Before $\text{WR} \uparrow$	100		ns	
t_{WD}	Data Hold Time After $\text{WR} \uparrow$	30		ns	Ports A & B
		30		ns	Port C

OTHER TIMINGS

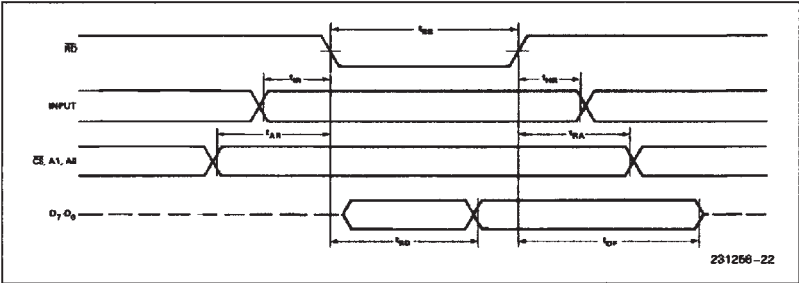
Symbol	Parameter	82C55A-2		Units Conditions	Test
		Min	Max		
t_{WB}	$WR = 1$ to Output		350	ns	
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	200		ns	
t_{ST}	$\overline{STB}$ Pulse Width	100		ns	
t_{PS}	Per. Data Before $\overline{STB}$ High	20		ns	
t_{PH}	Per. Data After $\overline{STB}$ High	50		ns	
t_{AD}	$\overline{ACK} = 0$ to Output		175	ns	
t_{KD}	$\overline{ACK} = 1$ to Output Float	20	250	ns	
t_{WOB}	$WR = 1$ to $\overline{OBF} = 0$		150	ns	
t_{AOB}	$\overline{ACK} = 0$ to $\overline{OBF} = 1$		150	ns	
t_{SIB}	$\overline{STB} = 0$ to $\overline{IBF} = 1$		150	ns	
t_{RIB}	$\overline{RD} = 1$ to $\overline{IBF} = 0$		150	ns	
t_{RIT}	$\overline{RD} = 0$ to $\overline{INTR} = 0$		200	ns	
t_{SIT}	$\overline{STB} = 1$ to $\overline{INTR} = 1$		150	ns	
t_{AIT}	$\overline{ACK} = 1$ to $\overline{INTR} = 1$		150	ns	
t_{WIT}	$WR = 0$ to $\overline{INTR} = 0$		200	ns	see note 1
t_{RES}	Reset Pulse Width	500		ns	see note 2

NOTE:

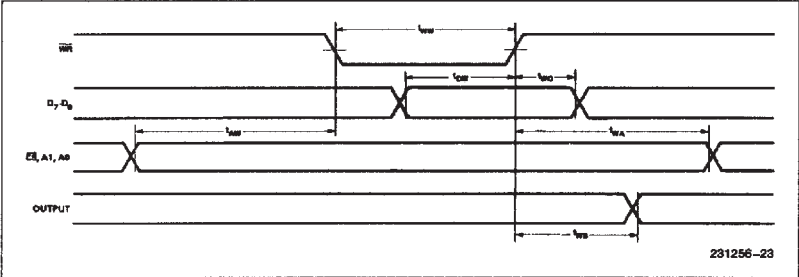
1. $\overline{INTR} \uparrow$ may occur as early as $WR \downarrow$.2. Pulse width of initial Reset pulse after power on must be at least 50 μ Sec. Subsequent Reset pulses may be 500 ns minimum.

WAVEFORMS

MODE 0 (BASIC INPUT)

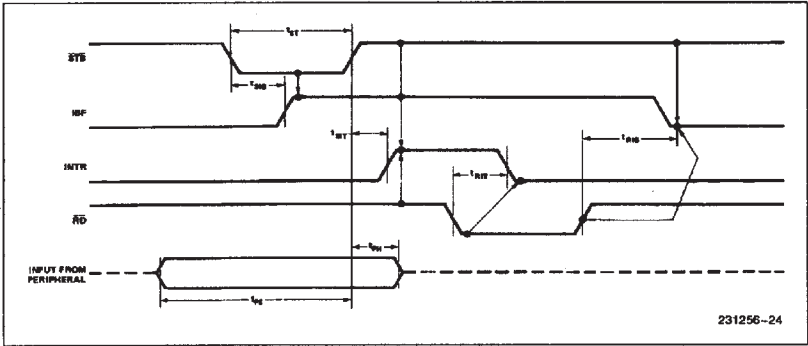


MODE 0 (BASIC OUTPUT)

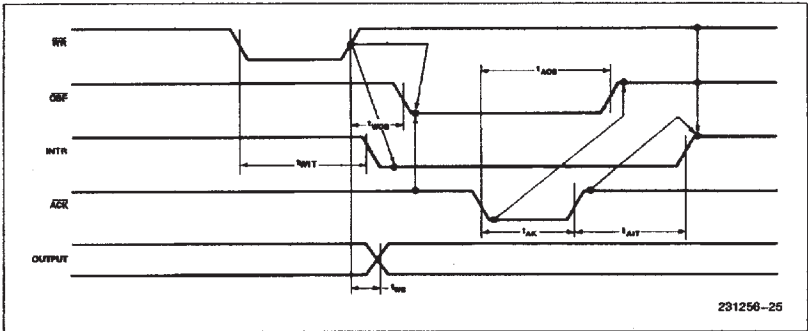


WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

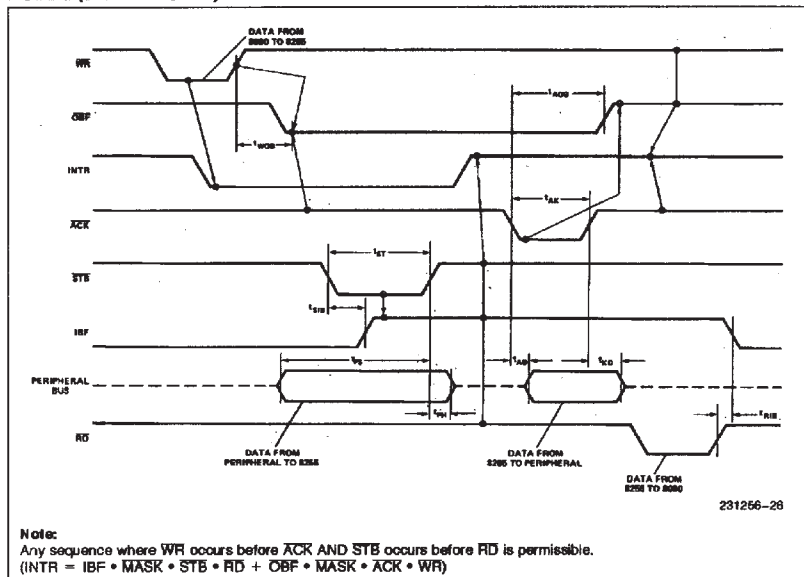


MODE 1 (STROBED OUTPUT)

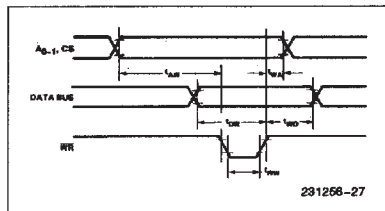


WAVEFORMS (Continued)

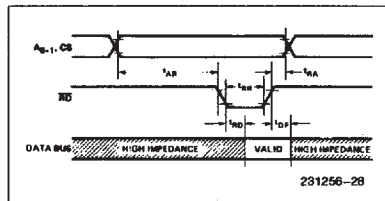
MODE 2 (BIDIRECTIONAL)



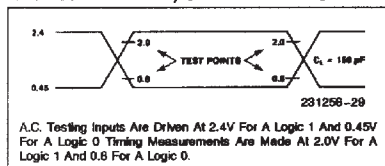
WRITE TIMING



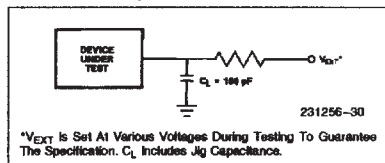
READ TIMING



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT



WARRANTY

Octagon Systems Corporation (Octagon), warrants that its standard hardware products will be free from defects in materials and workmanship under normal use and service for the current established warranty period. Octagon's obligation under this warranty shall not arise until Buyer returns the defective product, freight prepaid to Octagon's facility or another specified location. Octagon's only responsibility under this warranty is, at its option, to replace or repair, free of charge, any defective component part of such products.

LIMITATIONS ON WARRANTY

The warranty set forth above does not extend to and shall not apply to:

1. Products, including software, which have been repaired or altered by other than Octagon personnel, unless Buyer has properly altered or repaired the products in accordance with procedures previously approved in writing by Octagon.
2. Products which have been subject to power supply reversal, misuse, neglect, accident, or improper installation.
3. The design, capability, capacity, or suitability for use of the Software. Software is licensed on an "AS IS" basis without warranty.

The warranty and remedies set forth above are in lieu of all other warranties expressed or implied, oral or written, either in fact or by operation of law, statutory or otherwise, including warranties of merchantability and fitness for a particular purpose, which Octagon specifically disclaims. Octagon neither assumes nor authorizes any other liability in connection with the sale, installation or use of its products. Octagon shall have no liability for incidental or consequential damages of any kind arising out of the sale, delay in delivery, installation, or use of its products.

SERVICE POLICY

1. Octagon's goal is to ship your product within 5 working days of receipt.
 2. If a product should fail during the warranty period, it will be repaired free of charge. For out of warranty repairs, the customer will be invoiced for repair charges at current standard labor and materials rates.
 3. Customers that return products for repairs, within the warranty period, and the product is found to be free of defect, may be liable for the minimum current repair charge.
-

RETURNING A PRODUCT FOR REPAIR

Upon determining that repair services are required, the customer must:

1. Obtain an RMA (Return Material Authorization) number from the Customer Service Department, 303-430-1500.
2. If the request is for an out of warranty repair, a purchase order number or other acceptable information must be supplied by the customer.
3. Include a list of problems encountered along with your name, address, telephone, and RMA number.
4. Carefully package the product in an antistatic bag. (Failure to package in antistatic material will VOID all warranties.) Then package in a safe container for shipping.
5. Write RMA number on the outside of the box.
6. For products under warranty, the customer pays for shipping to Octagon. Octagon pays for shipping back to customer.
7. Other conditions and limitations may apply to international shipments.

NOTE: PRODUCTS RETURNED TO OCTAGON FREIGHT COLLECT OR WITHOUT AN RMA NUMBER CANNOT BE ACCEPTED AND WILL BE RETURNED FREIGHT COLLECT.

RETURNS

There will be a 15% restocking charge on returned product that is unopened and unused, if Octagon accepts such a return. Returns will not be accepted 30 days after purchase. Opened and/or used products, non-standard products, software and printed materials are not returnable without prior written agreement.

GOVERNING LAW

This agreement is made in, governed by and shall be construed in accordance with the laws of the State of Colorado.

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